REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Final Office Action of July 14, 2003 has been received and its contents carefully reviewed.

In the Final Office Action dated July 14, 2003, the Examiner rejected claims 1-26 under 35 U.S.C. §102(e) as being anticipated by Moon (U.S. Pat. No. 5,793,346). The rejection is traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1-26 under 35 U.S.C. § 102(e) as being anticipated by Moon is respectfully traversed and reconsideration is requested.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "level shifting means for receiving a power supply and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off." The cited references including Moon, do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claims 2-8, which depend from claim 1, are also allowable over the cited references.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on." The cited references including Moon, do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claim 10, which depends from claim 9, are also allowable over the cited references.

Claim 11 is allowable over the cited references in that claim 11 recites a combination of elements including, for example, "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output." The cited references including Moon, do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claims 12-18, which depend from claim 11, are also allowable over the cited references.

Claim 19 is allowable over the cited references in that claim 19 recites a combination of elements including, for example, "a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output." The cited references including Moon, do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claims 20-26, which depend from claim 19, are also allowable over the cited references.

To anticipate a claim, each and every element of the claim must be found, either expressly or implicitly, in a single prior art reference. See M.P.E.P. § 2131.

The Examiner cites Moon as teaching

> "a screen clearing circuit 40 connected at an input to the gate driving circuit 10 wherein the controller 30 controls gate driving circuit 10, which supplies gate on/off voltages sequentially through the gate lines to the thin film transistors 70 (column 4, lines 12-23, figure 6 at 10, 30). Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50) wherein the screen clearing circuit 40 is connected to the Voff output of gate on/off generator 50 (column 4, lines 25-26). When the external power is disconnected, the screen clearing circuit 40 operates to discharge the storage capacitors 80 connected to the gate lines (column 4, lines 27-29)." (Office Action at 3.)

Accordingly, Applicants respectfully submit, however, Moon does not teach or suggest at least the aforementioned claimed elements at least with respect to claims 1, 9, 11, and 19. To reiterate, claim 1 requires, among other elements "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on...," claim 9 requires, among other elements "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on," claim 11 requires, among other elements "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output," and claim 19 requires, among other elements "a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output."

Applicants respectfully submit Moon teaches at column 2, lines 60-65, "FIG. 4 shows a screen clearing circuit 40... The screen clearing circuit 40 is connected to each gate line in the TFT LCD ... [and] ...is inactive when external power VDD is being applied, but when the VDD is shut off, the circuit operates to discharge the support capacitor Cst." At column 4, lines 12-14 Moon states "FIG. 6 shows the screen clearing circuit 40 connected at an input to the gate driving circuit 10 as opposed to the direct connection to the gate lines shown in FIG. 4."

In view of the disclosure of Moon, the screen clearing circuit 40 operates to discharge the support capacitor Cst, presumably turning the TFTs 70 on when no external power VDD is applied. In further view of Moon, the screen clearing circuit 40 operates substantially the same regardless of where its output is arranged. Accordingly, Applicants respectfully submit Moon is silent as to at least the aforementioned combination of claimed elements. While

FIG. 6 illustrates the screen clearing circuit connected to an output of the gate on/off generator 50, Moon remains silent as to any teaching or suggestion about the components of the gate on/off generator 50 as well as any teaching or suggestion as to whether the gate on/off generator 50 generates, for example a gate-off voltage upon applying the external power VDD.

According to M.P.E.P. § 707.07(f), where Applicants traverse any rejection, the Examiner should, upon repeating the rejection, answer the substance of the Applicants' argument.

In both the present Request for Reconsideration and Reply Under 37 CFR § 1.111 mailed on May 6, 2003, Applicants argued Moon did not teach or suggest at least the aforementioned claimed elements at least with respect to claims 1, 9, 11, and 19. In response to the Applicants argument that Moon failed to teach or suggest "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off," as required by claim 1, or "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on," as required by claim 9, the Examiner asserted the inventions defined in claims 1 and 9 were met by Moon because Moon taught

> "...a screen clearing circuit 40 is connected at an input to the gate driving circuit 10 such that controller 30 controls gate driving circuit 10, which supplies gate on/off voltages sequentially through the gate lines to the thin film transistors 70 (column 4, lines 12-23, figure 6 at 10, 30). Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50)." (Office Action at 4.)

Applicants respectfully submit, however, that by merely restating the substance of the rejection applied to claims 1 and 9, the Examiner has not answered the substance of the Applicants previous and present arguments. Assuming *arguendo* that the Examiner's interpretation of Moon, as cited above, is correct, Moon still fails to teach or suggest at least the aforementioned independently claimed elements (e.g., "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off" and "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on").

Absent any evidentiary support, Applicants respectfully submit the screen clearing circuit 40 or the gate on/off generator 50 disclosed by Moon, either singly or in combination, cannot be reasonably interpreted to read on "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off" or "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on," as recited in the claims. In the absence of any evidentiary support or logical reasoning provided by the Examiner, Applicants respectfully submit Moon fails to anticipate the inventions defined by claims 1 and 9.

In response to the Applicants argument that Moon failed to teach or suggest "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output," as required by claim 11 or "a gate-off voltage generator having a transistor connected between a first voltage source and a

second voltage source to generate a gate-off voltage at an output," as required by claim 19, the Examiner asserted the inventions defined in claims 11 and 19 were met by Moon because Moon taught

> "...a gate on/off generator 50 generates Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50). This facilitates the elimination of residual image improves the quality of TFT LCDs" (Office Action at 4.)

Applicants respectfully submit, however, that by merely restating the substance of the rejection applied to claims 11 and 19, the Examiner has not answered the substance of the Applicants previous and present arguments. Assuming *arguendo* that the Examiner's interpretation of Moon, as cited above, is correct, Moon still fails to teach or suggest at least the aforementioned independently claimed elements (e.g., "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output" and "a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output").

Absent any evidentiary support, Applicants respectfully submit the gate on/off generator 50 disclosed by Moon cannot be reasonably interpreted to read on "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output" or "a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output," as recited in the claims. Moreover, Applicants respectfully submit Moon is completely silent as to any teaching or suggestion that the gate on/off generator 50 includes transistors connected between first and second voltage sources to

generate gate-off voltages. In the absence of any evidentiary support or logical reasoning provided by the Examiner, Applicants respectfully submit Moon fails to anticipate the inventions defined by claims 11 and 19.

Applicants believe the application is in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

MCKENNA LONG & ALDRIDGE, LLP

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By _____
Eric J. Nuss
Registration No.: 40,106

1900 K Street, N.W.
Washington, D.C. 20006
Telephone No.: (202) 496-7500
Facsimile No.: (202) 496-7756